REMARKS

Claims 1-18 and 25-44 are pending in the present application.

In the office action mailed June 30, 2005 (the "Office Action"), the Examiner objected to the specification for informalities. The Examiner further rejected claims 1-4, 6-8, 11-16, 25-30, 32-36, 38, 39, and 44 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,069,038 to Hashimoto *et al.* (the "Hashimoto patent"). Claims 5, 9, 10, 17, 18, 31, 37, and 40-43 were also rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over the Hashimoto patent in view of U.S. Patent No. 5,320,975 to Cederbaum *et al.* (the "Cederbaum patent").

With respect to the Examiner's objection to the specification, the specification has been amended as suggested by the Examiner. Consequently, the objection to the specification should be withdrawn.

As previously mentioned, claims 1-4, 6-8, 11-16, 25-30, 32-36, 38, 39, and 44 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Hashimoto patent.

Amended claims 1, 6, 11, 25, 26, 32, 38, and 44 are patentably distinct from the Hashimoto patent because the Hashimoto patent fails to disclose the combination of limitations recited by the respective claim. For example, with respect to claim 1, the Hashimoto patent fails to disclose a method for making a semiconductor structure in a substrate having an array area and a periphery area that includes forming openings by etching a nonconductive layer and a stopping layer wherein the openings expose a polycrystalline silicon layer of the transistor in the array area and the transistor in the periphery area.

In reviewing the material in the Hashimoto patent cited by the Examiner, forming openings by etching a nonconductive layer and a stopping layer wherein the openings expose a polycrystalline silicon layer of the transistor in the periphery area is not disclosed. The Hashimoto patent describes three embodiments of a method for forming a semiconductor device that includes DRAM cells, SRAM cells, and logic circuits. Figures 3-47 illustrate cross-sectional views for the three different sections included in the semiconductor device, namely, the left portion of each figure illustrates formation of the DRAM cells, the middle portion illustrates formation of the logic circuits, and the right portion illustrates formation of the SRAM cells. The process for the first embodiment is illustrated by Figures 3-28, the process for the second

embodiment is illustrated by Figures 30-39, and the process for the third embodiment is illustrated by Figures 40-47.

The first embodiment of the method described in the Hashimoto patent provides the benefit of having word lines for the DRAM array covered with a layer of silicon nitride, while the gates for the transistors of the logic circuit region and the SRAM array remain uncovered by the silicon nitride layer. The second embodiment has the benefit of providing relatively thick layers of silicon nitride over the gates and on the sidewalls of the gates in the DRAM and SRAM arrays as well as for the logic circuit region. This structure allows for the use of a self-aligned etch process during the formation of a contact in the logic circuit region that is aligned with a gate and an isolation structure. The third embodiment provides the benefit of forming the same basic structure as in the second embodiment, but with the added benefit of forming a polysilicon silicide layer on the gates concurrently with the formation of silicide on the active regions of the DRAM and SRAM arrays and the logic circuit region. The completed structures of the three different embodiments shown in Figures 28, 39, and 47 fail to illustrate exposing a polysilicon layer of a transistor in at least one of the array or periphery by forming and opening through a nonconductive layer and a stopping layer.

Claims 6, 11, 25, 26, 32, 38, and 44 include limitations that are not disclosed in the Hashimoto patent, as previously discussed. With respect to claim 6, the Hashimoto patent fails to disclose a method for making a semiconductor structure in a semiconductor substrate having an array and a periphery that includes removing the portions of the array and the periphery that are marked to expose a polycrystalline silicon layer of the gate and source/drain of the memory cell in the array and to expose the gate of the transistor in the periphery. With respect to claim 11, the Hashimoto patent fails to disclose a method for making a semiconductor structure in a substrate having an array and a periphery including photolithographing to mask portions of gates in the array and the periphery, the gates including a polycrystalline silicon layer and further dry-etching the portions of the array and the periphery until stopped by the stopping layer to expose a portion of the polycrystalline layer of at least one of the gates in the array and the periphery. With respect to claim 25, the Hashimoto patent fails to disclose a method for making a semiconductor structure in a periphery including forming a trench having a depth defined by etching the nonconductive layer until the act of etching stops when the stopping layer

is etched away to expose at least a portion of the single polycrystalline line. With respect to claim 26, the Hashimoto patent fails to disclose a method for strapping a semiconductor device in a periphery including forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench and expose at least a portion of the dual-doped polycrystalline silicon line.

With respect to claim 32, the Hashimoto patent fails to disclose a method for forming a routing in a periphery area of a semiconductor structure that includes forming from a nonconductive stack a first trench that superjacently abuts along a substantial length of a first gate stack in the periphery and further forming a second trench that superjacently abuts a second gate stack in the periphery, the first and second gate stacks including a polycrystalline silicon layer, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trenches and expose at least a portion of the polycrystalline silicon layer of the second gate stack.

With respect to claim 38, the Hashimoto patent fails to disclose a method for forming a contact to an active region in a periphery of a semiconductor structure that includes forming from a nonconductive stack a first an opening that abuts an active region in the periphery and further forming a second opening that abuts a gate stack in the periphery having a polycrystalline silicon layer, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench and expose at least a portion of the active region and at least a portion of the polycrystalline silicon layer.

With respect to claim 44, the Hashimoto patent fails to disclose a method for making semiconductor structures on a substrate having an array area and a periphery area that includes forming from a nonconductive stack a number of openings to expose a number of semiconductor structures in the array area and in the periphery area, the nonconductive stack including a stopping layer to stop an etching process once etched away to define the bottom of each opening and expose a portion of a polycrystalline silicon layer for at least one of the semiconductor structures in the array area and in the periphery area.

For the foregoing reasons, claims 1, 6, 11, 25, 26, 32, 38, and 44 are patentably distinct from the Hashimoto patent. Claims 2-4, which depend from claim 1, claims 7 and 8, which depend from claim 6, claims 12-16, which depend from claim 11, claims 27-30, which depend from claim 26, claims 33-36, which depend from claim 32, and claim 39, which depends from claim 38 are similarly patentably distinct from the Hashimoto patent based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claims 1-4, 6-8, 11-16, 25-30, 32-36, 38, 39, and 44 under 35 U.S.C. 102(b) should be withdrawn.

As previously mentioned, claims 5, 9, 10, 17, 18, 31, 37, and 40-43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Hashimoto patent in view of the Cederbaum patent.

Claims 5, 9, 10, 17, 18, 31, 37, and 40-43 are patentable over the Hashimoto patent in view of the Cederbaum patent because the combined teachings fail to teach or suggest the combination of limitations recited by the respective claim.

The Cederbaum patent has been cited as disclosing forming an opening and filling the opening with a metallization layer which comprises a silicide compound, a barrier layer, and a conductive layer. *See* the Office Action, page 4. Even if it is assumed for the sake of argument that the Examiner's characterization of the Cederbaum patent is accurate, the Cederbaum patent fails to make up for the deficiencies of the Hashimoto patent, as previously discussed with respect to claims 1, 6, 11, 25, 26, 32, 38, and 44.

For the foregoing reasons, claims 5, 9, 10, 17, 18, 31, and 40-43 are patentable over the Hashimoto patent in view of the Cederbaum patent. Consequently, the rejection of claims 5, 9, 10, 17, 18, 31, and 40-43 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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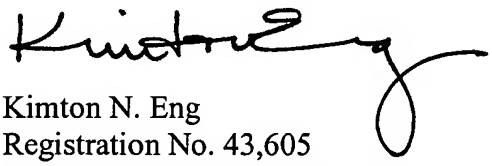

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